

TRANSMITTAL LETTER TO THE UNITED STATES

DESIGNATED/ELECTED OFFICE (DO/EO/US)

CONCERNING A FILING UNDER 35 U.S.C. 371

KSN0012

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR

09/806401

INTERNATIONAL APPLICATION NO.

PCT/DE99/03247

INTERNATIONAL FILING DATE

08 October 1999

PRIORITY DATE CLAIMED

09 October 1998

TITLE OF INVENTION

ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION AND CORRESPONDING PRODUCTION METHOD

APPLICANT(S) FOR DO/EO/US

Harry Hedler, Gregor Feiertag, Peter Deml, and Franz Petter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
  - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☒ has been transmitted by the International Bureau.
  - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
  - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☐ have been transmitted by the International Bureau.
  - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
  - d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☐ Other items or information:

Check No. in the amount of \$860.00, Copy of Change of Applicant

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR <div style="font-size: 1.5em; font-weight: bold;">07/806401</div>	INTERNATIONAL APPLICATION NO. <div style="font-weight: bold;">PCT/DE99/03247</div>	ATTORNEY'S DOCKET NUMBER <div style="font-weight: bold;">KSN0012</div>
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21. The following fees are submitted..

**BASIC NATIONAL FEE ( 37 CFR 1.492 (a) (1) - (5) ) :**

☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO ..... **\$1,000.00**

☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... **\$860.00**

☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... **\$710.00**

☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... **\$690.00**

☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) ..... **\$100.00**

**ENTER APPROPRIATE BASIC FEE AMOUNT =**

**CALCULATIONS PTO USE ONLY**

**\$860.00**

**\$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	9 - 20 =	0	x \$18.00	<b>\$0.00</b>
Independent claims	1 - 3 =	0	x \$80.00	<b>\$0.00</b>
Multiple Dependent Claims (check if applicable).				<input type="checkbox"/> <b>\$0.00</b>
<b>TOTAL OF ABOVE CALCULATIONS</b>				<b>= \$860.00</b>
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable).				<input type="checkbox"/> <b>\$0.00</b>
<b>SUBTOTAL</b>				<b>= \$860.00</b>
Processing fee of \$130.00 for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492 (f)).				<input type="checkbox"/> 20 <input type="checkbox"/> 30 + <b>\$0.00</b>
<b>TOTAL NATIONAL FEE</b>				<b>= \$860.00</b>
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable).				<input type="checkbox"/> <b>\$0.00</b>
<b>TOTAL FEES ENCLOSED</b>				<b>= \$860.00</b>
				Amount to be refunded <b>\$</b>
				charged <b>\$</b>

☒ A check in the amount of **\$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \_\_\_\_\_ to cover the above fees.  
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-0387** A duplicate copy of this sheet is enclosed.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

**SEND ALL CORRESPONDENCE TO:**

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SIGNATURE \_\_\_\_\_

**Eric J. Groen**

NAME \_\_\_\_\_

**32,230**

REGISTRATION NUMBER \_\_\_\_\_

**March 30, 2001**

DATE \_\_\_\_\_

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Harry Hedler, Gregor Feiertag,  
Peter Deml, and Franz Petter

Filed: PCT/DE99/03247 October 8, 1999

For: ELECTRONIC MODULE, ESPECIALLY A  
MULTICHIP MODULE, WITH MULTI-LAYER  
METALLIZATION AND CORRESPONDING  
PRODUCTION METHOD

Commissioner for Patents and Trademarks  
Washington DC 20231

Dear Sir:

**PRELIMINARY AMENDMENT**

In the above-mentioned PCT application, please accept the enclosed application under the national stage pursuant to 35 USC § 371 and amend the application as follows:

In the Claims:

Please replace claims 1-8 of the application with claims 1-9 as follows:

1. An electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module through for contacting and integration of the module to a next higher assembly group level, the bottom side of the multilayer wiring constituting directly, without additional wiring substrate, the bottom side of the module, the component side of the multilayer wiring adhering to the hermetic case with

its portions that are free from components, said hermetic case being formed by plastics overmolding, and in that the multilayer wiring has a height of less than approximately 100  $\mu\text{m}$ .

2. A module according to claim 1, wherein the multilayer wiring is constituted by a sequence of structured metal planes which are electrically separated from each other by insulating layers and between which purposeful electric connections are established through vias.

3. A module according to claim 1, wherein solderable material is applied to the contact pads on the bottom side of the multilayer wiring, electrically connected to the component level through vias, for establishing contact with the next assembly group level.

4. A module according to claim 3, wherein the solderable material is applied in the form of solder balls

5. A method of making an electronic module according to claim 1, in which

- a multilayer wiring having contact pads on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate of rigid material,

- IC components and additional electronic components, respectively, are electrically and mechanically connected to the component level of the multilayer wiring,

the component side of the multilayer wiring is provided with a hermetic case adhering in the portions thereof that are free from components,

- the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring which constitutes the bottom side of the module, is exposed, and

said hermetic case is formed by unilateral plastics overmolding.

6. A method according to claim 4, wherein, prior to removal of the particular metallic substrate material in portions located underneath the contact pads, pits are etched into the wiring substrate from the bottom side, with solderable material being introduced into said pits thereafter.

7. A method according to claim 4, wherein the removal of the particular metallic substrate material takes place by dissolution of the same.

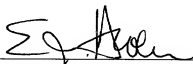
8. A method according to claim 7, wherein the dissolution takes place by wet chemical etching.

9. A method according to claim 4, wherein the removal of the substrate material takes place by stripping the wiring substrate from the multilayer wiring.

### REMARKS

Applicants respectfully request that the above preliminary amendment be entered, and that the fees due herewith are calculated using the new claims, not the claims of the PCT application.

Respectfully submitted,



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1/12

## Specification

- 5 Electronic Module, in Particular a Multichip Module,  
Comprising a Multilayer Wiring and Method of Making the  
Same.

10 The invention relates to an electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module  
15 through which contacting and integration of the module to a next higher assembly group level can be established.

The invention moreover relates to a method of making an  
20 electronic module, in particular a multichip module, comprising a multilayer wiring.

The increasing reduction in size and growing speed of integrated circuits meets with increasing demands on the  
25 extension and connection technology thereof. Multichip modules have been known for some time through which an intermediate carrier substrate with high wiring density, HDI (High Density Interconnect), is introduced into the hierarchy of the system structure as an additional  
30 level. Typical in this respect is the use of a plurality of unpackaged chips as well as a high area coverage of the multichip substrate. A similar known new development relates to the chip size package (CSP) in which a single unpackaged chip is applied to an intermediate carrier  
35 substrate which is hardly larger than the chip area and in which the space-saving contacting to the next architectural level directly under the chip area is utilized.

40 The essential features of today's packages for single-  
 chip or multichip applications are the lateral dimen-  
 sion, the construction height, the heat dissipation and  
 the pitch in the next architectural level. The utiliza-  
 tion of the known quad flat pack (QFP) packages, in ad-  
 dition to the relatively low degree of chip coverage  
 45 (chip area/component area) and the relatively high con-  
 struction height, involves the additional disadvantage  
 of the transition to extremely small pitches on the  
 motherboard with high pincount of the chips. There is  
 also known an additional package type, the ball grid ar-  
 50 rays (BGA). In case of these, small solder balls applied  
 over the area or in sheet-like manner on the bottom side  
 of the module in a relatively coarse grid pattern, con-  
 stitute the terminals. By means of BGA constructions,  
 the arrangement of the contacts in sheet-like manner as-  
 55 sists in mitigating the problems concerning the pitch,  
 and the construction height can be reduced in principle.  
 However, the manufacture of conventional laminate/plas-  
 tics interconnects, in particular for high-density wir-  
 60 ings, results in technical detours and disadvantageous  
 product properties. In total, the current situation pre-  
 sents itself as follows:

65 The technologies of circuit board production render pos-  
 sible wiring substrates permitting electric through-con-  
 tacting from the chip side to the bottom side by means  
 of plated-through holes that can be made in relatively  
 simple manner. They are less advantageous as regards the  
 production of constructional shapes of small lateral di-  
 mensions, in particular for multichip modules, as the  
 70 wiring densities are too low. Furthermore, in particular  
 vias between the conductive track levels are not posi-  
 tioned in sufficiently exact manner due to the shrinkage  
 of the laminate materials. There are left uncertainties  
 of typically up to 200  $\mu\text{m}$ , and this is brought to regis-



75 tration by a coarser design of the structure around the  
via (land). Due to the shrinkage, high-density wiring  
substrates can be realized only if the production is not  
carried out on the inexpensive large panels, for example  
of 600 x 600 mm, but on extremely small ones, for exam-  
80 ple of 150 x 150 mm. Large-format production in circuit  
board technology thus involves high costs comparable to  
those in thin-film technology.

85 The technologies of thin-film production permit high  
wiring densities due to their processes employing fine  
structures, and there is no shrinkage problem due to the  
rigid substrate materials (the substrate proper for the  
multilayer wiring consists of ceramic, silicon, glass or  
metal). However, there are problems arising with other  
aspects of this technology, in particular as regards the  
90 cost-intensive detours, such as drilling or punching  
holes in the rigid core materials, adjustment problems,  
metallization of the holes, etc., as necessary in real-  
izing the electrical connection from the substrate top  
side to the substrate bottom side. In addition thereto,  
95 the density of the plated-through holes is restricted by  
the substrate thickness and the respective technology  
for making the hole. In general, there is poor compati-  
bility between the technology of substrates with holes  
100 on the one hand and processes in thin-film technique,  
for example spin coating, on the other hand. Finally,  
there is also a high risk of breakage of the substrates  
in the thin-film process which moreover does not permit  
a simple change to inexpensive large-format production,  
105 either.

It is the object of the present invention to provide an  
improved module of the type indicated at the outset,  
having in particular a reduced construction height, and  
110 to indicate a method of making the same.

With a module of the type indicated at the outset, this object is met in that the component side of the multilayer wiring adheres to the hermetic case with its portions that are free from components, and in that the bottom side of the multilayer wiring having a height of less than approx. 100  $\mu\text{m}$ , directly, i.e. without additional wiring substrate, constitutes the bottom side of the module.

With a method of the type indicated at the outset, the object is met in that a multilayer wiring having contact pads on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate of rigid material, that IC components and additional electronic components, respectively, are electrically and mechanically connected to the component level of the multilayer wiring, that the component side of the multilayer wiring is provided with a hermetic case adhering in the portions thereof that are free from components, and in that the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring, which constitutes the bottom side of the module, is exposed.

Further developments of the invention are subject matter of the dependent claims.

The invention will be elucidated in more detail herein-after by way of embodiments in connection with the drawing figures in which

Figs. 1A to 1D show cross-sectional side views of successive stages of the manufacturing process according to the invention in a first embodiment,

Figs. 2A to 2F show corresponding views of another embodiment,

150 Figs. 3A to 3F show corresponding views in a further embodiment.

The invention achieves the desired improvements in that not only the processes of the interconnect production proper are taken into consideration, but in that the overall process for making a BGA standard package is incorporated in the rationalization and restructuring of the process sequences according to the invention and thus of the module itself. According to the invention, it is possible to produce ultra-thin modules although the utilization of the advantages of thin-film technique, i.e. in particular the use of rigid substrate materials or materials of high temperature stability (up to 400 °C) is maintained on the one hand, whereas on the other hand a high wiring density can be achieved in unrestricted manner and large-size panels, for example 400 x 400 mm, can be used for the production. In addition thereto, there is the advantage that process steps can be dispensed with.

170 Fig. 1A shows a metallic wiring substrate 1 having already applied on the top side thereof the interconnect proper, i.e. the multilayer wiring 2, which is constituted by a sequence of structured metal planes or levels that are electrically separated from each other by insulating layers and between which purposeful electric connections are established through vias. Suitable substrate materials are, for example, copper or aluminium. It is of crucial importance that the multilayer wiring 2 actually is applied on the substrate top side only and that there are no plated-through holes made from the top side to the bottom side of wiring substrate 1. Fig. 1 shows a module in which, compared with Fig. 1A, two additional production steps have been carried out, namely mechanical and electrical connection of one or more

chips 3 and, optionally, of additional electronic components to the component side of the multilayer wiring 2, for example by chip and wire bond technique or flip chip technique, with the equipped system being then brought  
 190 into the configuration of a standard package by unilateral plastics molding (overmold), cp. case 4. The largest part of the component area, i.e. of the top side of the multilayer wiring 2, is free from components so that the casting or adhesive compound 4 applied can establish  
 195 sufficient adhesive areas 5 towards the multilayer wiring 2. In particular, the usual casting compounds may be employed as these are compatible anyway, i.e. capable of adhering, to the insulating materials used as uppermost layer of the multilayer wiring 2, such as polyimide,  
 200 PBO, BCB or ormocere.

Fig. 1C shows a module in which the next process step, the removal of the substrate material 1, has already been carried out. This can be achieved, for example, by  
 205 dissolution of the substrate material, in particular by wet chemical etching in one of the etch plants usual in the trade, as used for example in high-integration semiconductor technology. Thereafter and due to this, the contact pads 6 on the bottom side of the multilayer wiring 2, which by means of vias and connections to the  
 210 conductive track system are to ensure the electrical contact of the components 3 of the module to the contacts of the next higher assembly group level, of course are exposed as well. As shown in Fig. 1D, this is usually followed by the application of solderable material,  
 215 in particular soldering balls 7, to the contact pads 6 for establishing contact to the module. A passivation layer 15 may be provided to permit easier testing of the module later on, cp. Fig. 1B. Basically, e.g. plastics  
 220 material is possible as substrate material as well.

While Figs. 2A and 2B correspond to the manufacturing steps according to Fig. 1A and 1B, Figs. 2C and 2F show embodiments differing therefrom. Fig. 2C shows the result of etching pits 8 into the substrate material from the bottom side, so that the contact locations, i.e. the contact pads 6 on the bottom side of the multilayer wiring 2 are exposed. Thereafter, solderable material 9 (e.g. SnPb) can be introduced into the pits 8 by electroplating, or solder balls 7 can be introduced into the pits 8 by standard processes, cp. Fig. 1D. Only thereafter is the removal of the wiring substrate 1 carried out, with modules according to Fig. 2E or 2F being the final result depending on the type of solder material 8, 9 chosen.

As an alternative to the removal of the substrate material by dissolution as described hereinbefore, another suitable possibility of separation consists in stripping the wiring substrate 1 from the multilayer wiring 2. This can be realized in particular by application of an intermediate layer between multilayer wiring 2 and wiring substrate 1. For example, a low melting point material, e.g. solder, or an adhesive is well suited, which at the end of the molding process permits separation of the module from the wiring substrate 1, for example, by means of an additional heat treatment step. Figs. 3A to 3E display a process sequence in which a solder layer 10 as intermediate layer is applied to the substrate material first, which then is covered with a structured insulating layer 11. According to Fig. 3C a structured metal plane 12 is made, which according to Fig. 3D is equipped with electronic components and covered by a hermetic case 4. Fig. 3E shows the final result after heating of the solder layer 10 and removal of the wiring substrate 1, with harmless residues of the solder layer 10 being left at the solder pads 10, and only there. Within the conductive track system of the multilayer

260 wiring 2, which in this special case permitting particularly inexpensive production consists of one single metal and one single insulating layer 12 and 11 only, the metal lands 13 and 14 are connected to each other. When an adhesive is used as intermediate layer, care should be taken that the same is as residue-free as possible, or post-cleaning should be provided for.

270 According to the invention, the result achieved consists in a module in the form of a BGA standard package having an extremely low assembly height, since the sole remaining multilayer wiring 2, the interconnect proper, has an assembly height of less than approx. 100  $\mu\text{m}$ , mostly even less than 60  $\mu\text{m}$ . Due to the fact that the chips 3 in thinned form typically have a height of approx. 300  $\mu\text{m}$  and the hermetic case 4 once more takes a similar height, minimum package heights (without balls) of approx. 600  $\mu\text{m}$  can be achieved according to the invention, whereas for example in laminate technology the known interconnect alone, i.e. the wiring substrate with the multilayer wiring arranged thereon has a height between 275 500  $\mu\text{m}$  and 1000  $\mu\text{m}$ .

## Translation of Amended Pages

## 5 Claims

1. An electronic module, in particular a multichip module, comprising a multilayer wiring having at least one IC component applied on the component side thereof, said module being unilaterally covered on the component side with a hermetic case, and comprising contact pads on the bottom side of the module through which contacting and integration of the module to a next higher assembly group level can be established, the bottom side of the multilayer wiring (2) constituting directly, i.e. without additional wiring substrate (1), the bottom side of the module, characterized in
- 20 that the component side of the multilayer wiring (2) adheres to the hermetic case (4) with its portions that are free from components, said hermetic case (4) being formed by plastics overmolding, and in that the multilayer wiring (2) has a height of less than approx. 100  $\mu\text{m}$ .
2. A module according to claim 1, characterized in that the multilayer wiring (2) is constituted by a sequence of structured metal planes (12) which are electrically separated from each other by insulating layers (11) and between which purposeful electric connections are established through vias.
3. A module according to claim 1 or 2, characterized in that, for establishing contact with the next assembly group level, solderable material

(7, 9), in particular solder balls (7), are applied to the contact pads (6) on the bottom side of the multilayer wiring (2) which are electrically connected to the component level through vias.

4. A method of making an electronic module according to claim 1, in which

- a multilayer wiring (1) having contact pads (6) on the bottom side thereof is applied only to the top side of a plate-shaped wiring substrate (1) of rigid material,
  - IC components and additional electronic components (3), respectively, are electrically and mechanically connected to the component level of the multilayer wiring (2),
  - the component side of the multilayer wiring (2) is provided with a hermetic case (4) adhering in the portions thereof that are free from components,
  - and the rigid substrate material is removed again thereafter and the bottom side of the multilayer wiring (2), which constitutes the bottom side of the module, is exposed,
- characterized in that said hermetic case is formed by unilateral plastics overmolding.

5. A method according to claim 4,

characterized in that, prior to removal of the in particular metallic substrate material in portions located underneath the contact pads (6), pits (8) are etched into the wiring substrate (1) from the bottom side, with solderable material (7, 9) being introduced into said pits (8) thereafter.

6. A method according to claim 4 or 5,



characterized in that the removal of the in particular metallic substrate material takes place by dissolution of the same.

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7. A method according to claim 6, characterized in that the dissolution takes place by wet chemical etching.

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8. A method according to claim 4 or 5, characterized in that the removal of the substrate material takes place by stripping the wiring substrate (1) from the multilayer wiring (2).

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1/4

FIG 1 A

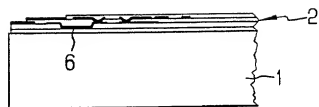


FIG 1 B

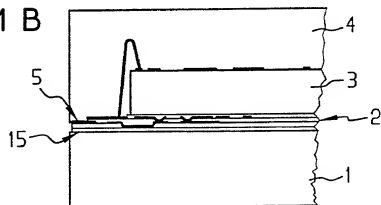


FIG 1 C

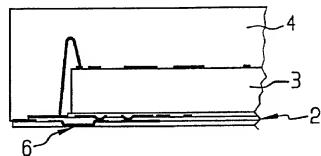
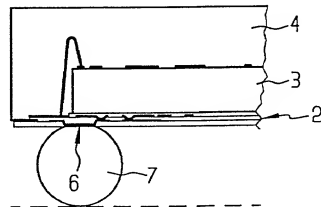


FIG 1 D



2/4

FIG 2 A

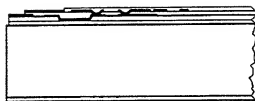


FIG 2 B

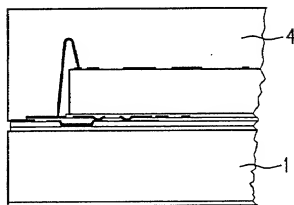
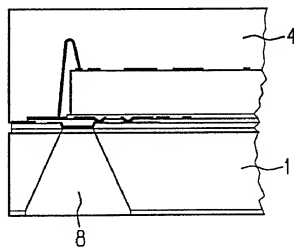


FIG 2 C



3/4

FIG 2 D

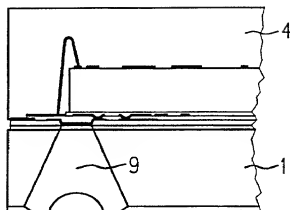


FIG 2 E

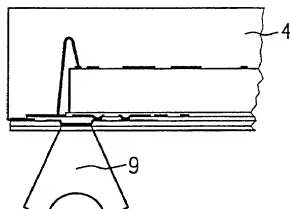
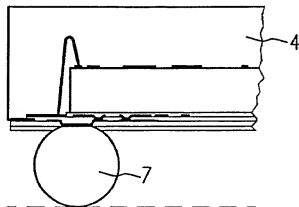


FIG 2 F





Docket No.  
KSN0012

# Declaration and Power of Attorney For Patent Application

## English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION**

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ as United States Application No. or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Prior Foreign Application(s)

Priority Not Claimed

DE 198 46 662.5	Germany	9 October 1998	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	
			<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	
			<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/DE99/03247

8 October 1999

Pending

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Status)  
(patented, pending, abandoned)

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Status)  
(patented, pending, abandoned)

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Status)  
(patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Eric J. Groen, 32,230  
 Gerard T. Gallagher, 39,679  
 Robert D. Null, 40,746  
 Daniel Tychonievich, 41,358  
 Deborah R. Beck, 37,370  
 Michael D. Beck, 32,722  
 Kevin R. Erdman, 33,687  
 John F. Hoffman, 26,280  
 Anthony Niewyk, 24,871  
 Nancy G. Tinsley, 37,098  
 Arthur R. Whale, 18,778

Send Correspondence to: Eric J. Groen  
Baker & Daniels  
205 West Jefferson Blvd., Suite 250  
South Bend, IN 46601

Direct Telephone Calls to: (name and telephone number)  
Eric J. Groen (219)234-4149

Full name of sole or first inventor <u>Harry Hedler</u>	
Sole or first inventor's signature	Date <u>30.05.01</u>
Residence <u>Pfarrgartenweg 50 A, D-81377 Munchen, Germany</u>	Jahnstrasse 8, D-82110 Germering <u>DEU</u>
Citizenship <u>German</u>	<u>Harry Hedler</u>
Post Office Address <u>Pfarrgartenweg 50 A, D-81377 Munchen, Germany</u>	Jahnstrasse 8, D-82110 Germering

Full name of second inventor, if any <u>Gregor Feiertag</u>	
Second inventor's signature	Date
Residence <u>Ruffinstrasse 22, D-80637 Munchen, Germany</u>	<u>DEU</u>
Citizenship <u>German</u>	
Post Office Address <u>Ruffinstrasse 22, D-80637 Munchen, Germany</u>	



30 Full name of third inventor, if any

Peter Deml

Third inventor's signature

Date

Residence

Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany DEX

Citizenship

German

Post Office Address

Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany

H-D Full name of fourth inventor, if any

Franz Petter

Fourth inventor's signature

Date

Residence

Hohenweg 20, D-85247 Schwabhausen, GermanyHohenweg 20, D-85247 Oberroth DEX

Citizenship

German

Post Office Address

Hohenweg 20, D-85247 Schwabhausen, GermanyHohenweg 20, D-85247 Oberroth

Full name of fifth inventor, if any

Fifth inventor's signature

Date

Residence

Citizenship

Post Office Address

Full name of sixth inventor, if any

Sixth inventor's signature

Date

Residence

Citizenship

Post Office Address

Docket No.  
KSN0012

# Declaration and Power of Attorney For Patent Application

## English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION**

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ as United States Application No. or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Prior Foreign Application(s)

Priority Not Claimed

DE 198 46 662.5  
(Number)  
  
(Number)  
  
(Number)

Germany  
(Country)  
  
(Country)  
  
(Country)

9 October 1998  
(Day/Month/Year Filed)  
  
(Day/Month/Year Filed)  
  
(Day/Month/Year Filed)

☐  
☐  
☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/DE99/03247

8 October 1999

Pending

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

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
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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 South Bend, IN 46601

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 Eric J. Groen (219)234-4149

Full name of sole or first inventor <b>Harry Hedler</b>	
Sole or first inventor's signature	Date
Residence <b>Pelargonicweg 50 A, D-81377 Munchen, Germany</b> Jahnstrasse 8, D-82110 Germering	
Citizenship <b>German</b>	
Post Office Address <b>Pelargonicweg 50 A, D-81377 Munchen, Germany</b> Jahnstrasse 8, D-82110 Germering	

Full name of second inventor, if any <b>Gregor Feiertag</b>	
Second inventor's signature 	Date May 27, 2007
Residence <b>Ruffinstrasse 22, D-80637 Munchen, Germany</b>	
Citizenship <b>German</b>	
Post Office Address <b>Ruffinstrasse 22, D-80637 Munchen, Germany</b>	

Full name of third inventor, if any <b>Peter Deml</b>	
Third inventor's signature	Date
Residence <b>Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany</b>	
Citizenship <b>German</b>	
Post Office Address <b>Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany</b>	

Full name of fourth inventor, if any <b>Franz Petter</b>	
Fourth inventor's signature	Date
Residence <b>Hohenweg 20, D-85247 Schwabhausen, Germany</b> <b>Hohenweg 20, D-85247 Oberroth</b>	
Citizenship <b>German</b>	
Post Office Address <b>Hohenweg 20, D-85247 Schwabhausen, Germany</b> <b>Hohenweg 20, D-85247 Oberroth</b>	

Full name of fifth inventor, if any	
Fifth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of sixth inventor, if any	
Sixth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Docket No.  
KSN0012

# Declaration and Power of Attorney For Patent Application

## English Language Declaration

As a below named inventor, I hereby declare that:

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**ELECTRONIC MODULE, ESPECIALLY A MULTICHIP MODULE, WITH MULTI-LAYER METALLIZATION**

the specification of which

(check one)

☒ is attached hereto.

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Priority Not Claimed

DE 198 46 662.5	Germany	9 October 1998	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	
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_____	_____	_____	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 103 of any United States provisional application(s) listed below:

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

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PCT/DE99/03247

8 October 1999

Pending

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
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 South Bend, IN 46601

Direct Telephone Calls to: (name and telephone number)  
**Eric J. Groen (219)234-4149**

Full name of sole or first inventor <b>Harry Hedler</b>	
Sole or first inventor's signature	Date
Residence <b>Pelargonienweg 50 A, D-81377 Munchen, Germany</b> Jahnstrasse 8, D-82110 Germering	
Citizenship <b>German</b>	
Post Office Address <b>Pelargonienweg 50 A, D-81377 Munchen, Germany</b> Jahnstrasse 8, D-82110 Germering	

Full name of second inventor, if any <b>Gregor Feiertag</b>	
Second inventor's signature	Date
Residence <b>Ruffinstrasse 22, D-80637 Munchen, Germany</b>	
Citizenship <b>German</b>	
Post Office Address <b>Ruffinstrasse 22, D-80637 Munchen, Germany</b>	



Full name of third inventor, if any <b>Peter Deml</b>	
Third inventor's signature	Date <b>6.7.01</b>
Residence <b>Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany</b>	
Citizenship <b>German</b>	
Post Office Address <b>Jagerweg 11, D-83620 Feldkirchen-Westerham, Germany</b>	
<i>Deml Pte</i>	

Full name of fourth inventor, if any <b>Franz Petter</b>	
Fourth inventor's signature	Date
Residence <b>Hohenweg 20, D-85247 Schwabhausen, Germany</b> <b>Hohenweg 20, D-85247 Oberroth</b>	
Citizenship <b>German</b>	
Post Office Address <b>Hohenweg 20, D-85247 Schwabhausen, Germany</b> <b>Hohenweg 20, D-85247 Oberroth</b>	

Full name of fifth inventor, if any	
Fifth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of sixth inventor, if any	
Sixth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

# Declaration and Power of Attorney For Patent Application

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(Number)

Germany

(Country)

9 October 1998

(Day/Month/Year Filed)

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(Number)

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☐

(Number)

(Country)

(Day/Month/Year Filed)

☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

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(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

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PCT/DE99/03147

8 October 1999

Pending

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
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(Application Serial No.)

(Filing Date)

(Status)  
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Full name of sole or first inventor Harry Redler	
Sole or first inventor's signature	
Date	
Residence Fahrgartenweg 56 A, D-81377 München, Germany Jahnstrasse 8, D-82110 Germering	
Citizenship German	
Post Office Address Fahrgartenweg 56 A, D-81377 München, Germany Jahnstrasse 8, D-82110 Germering	

Full name of second inventor, if any Gregor Felertag	
Second inventor's signature	
Date May 23, 2007	
Residence Ruffinstrasse 22, D-80637 München, Germany	
Citizenship German	
Post Office Address Ruffinstrasse 22, D-80637 München, Germany	

Full name of third inventor, if any	
Peter Deml	
Third inventor's signature	Date 6.7.01
Residence Jägerweg 11, D-83620 Feldkirchen-Westerham, Germany	
Citizenship German	
Post Office Address Jägerweg 11, D-83620 Feldkirchen-Westerham, Germany	
<i>Deml PE</i>	

Full name of fourth inventor, if any	
Franz Petter	
Fourth inventor's signature	Date 5.10.2001
Residence Hohenweg 20, D-85247 Schwabhausen, Germany Hohenweg 20, D-85247 Oberroth	
Citizenship German	
Post Office Address Hohenweg 20, D-85247 Schwabhausen, Germany Hohenweg 20, D-85247 Oberroth	
<i>Petter FR</i>	

Full name of fifth inventor, if any	
Fifth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of sixth inventor, if any	
Sixth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	